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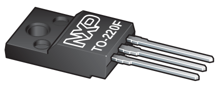


PSMN9R5-100XS

N-channel 100V 9.6 mΩ standard level MOSFET in TO220F (SOT186A)

Rev. 3 — 6 March 2012 Product data sheet

1. Product profile

1.1 General description

Standard level N-channel MOSFET in TO220F (SOT186A) package qualified to 175C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

1.2 Features and benefits

- High efficiency due to low switching and conduction losses
- Isolated package
- Suitable for standard level gate drive

1.3 Applications

- AC-to-DC power supply equipment
- Motor control
- Server power supplies
- Synchronous rectification

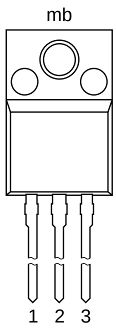
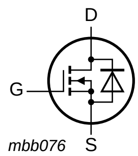
1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 175$ °C	-	-	100	V
I_D	drain current	$T_{mb} = 25$ °C; $V_{GS} = 10$ V; see Figure 1	-	-	44.2	A
P_{tot}	total power dissipation	$T_{mb} = 25$ °C; see Figure 2	-	-	52.6	W
Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10$ V; $I_D = 10$ A; $T_j = 25$ °C; see Figure 12; see Figure 13	-	8.15	9.6	mΩ
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 10$ V; $I_D = 10$ A; $V_{DS} = 50$ V; see Figure 14; see Figure 15	-	24.3	-	nC
$Q_{G(tot)}$	total gate charge		-	81.5	-	nC
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10$ V; $T_{j(init)} = 25$ °C; $I_D = 44.2$ A; $V_{sup} \leq 100$ V; unclamped; $R_{GS} = 50$ Ω; see Figure 3	-	-	260	mJ

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain		
3	S	source		
mb		mounting base; isolated		

SOT186A (TO-220F)

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN9R5-100XS	TO-220F	plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3-lead TO-220 "full pack"	SOT186A

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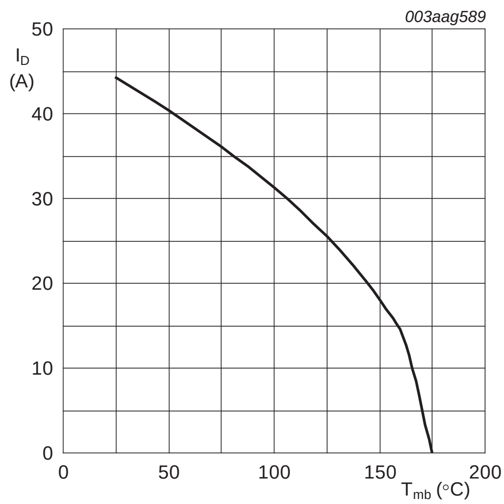
4. Limiting values

Table 4. Limiting values

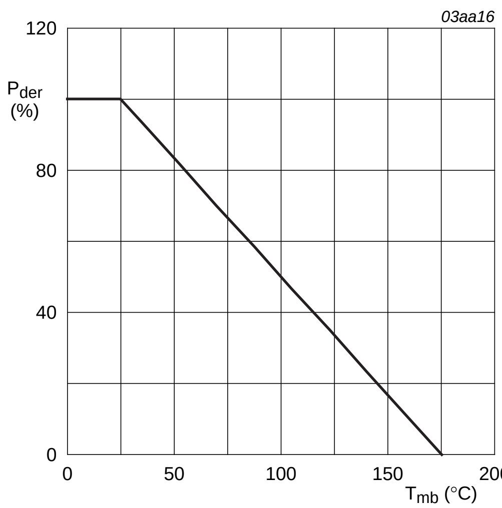
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 175$ °C	-	100	V
V_{DGR}	drain-gate voltage	$T_j \geq 25$ °C; $T_j \leq 175$ °C; R_{GS} = 20 kΩ	-	100	V
V_{GS}	gate-source voltage		-20	20	V
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; see Figure 1	-	44.2	A
		V_{GS} = 10 V; T_{mb} = 100 °C; see Figure 1	-	31.3	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10$ µs; T_{mb} = 25 °C; see Figure 4	-	177	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; see Figure 2	-	52.6	W
T_{stg}	storage temperature		-55	175	°C
T_j	junction temperature		-55	175	°C
$T_{sld(M)}$	peak soldering temperature		-	260	°C
Source-drain diode					
I_S	source current	T_{mb} = 25 °C	-	43.8	A
I_{SM}	peak source current	pulsed; $t_p \leq 10$ µs; T_{mb} = 25 °C	-	177	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; I_D = 44.2 A; $V_{sup} \leq 100$ V; unclamped; R_{GS} = 50 Ω; see Figure 3	-	260	mJ



$$V_{GS} \geq 10V$$

Fig 1. Continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ C)}} \times 100\,\%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature

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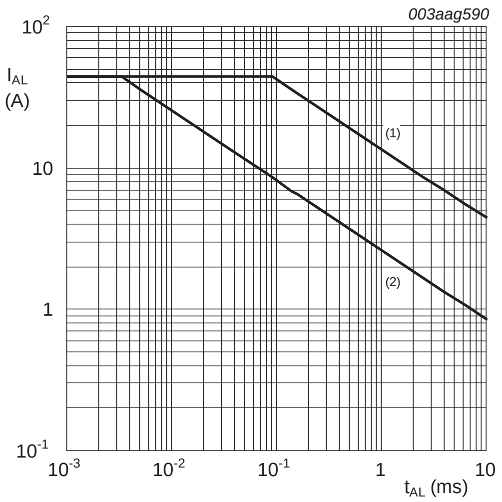
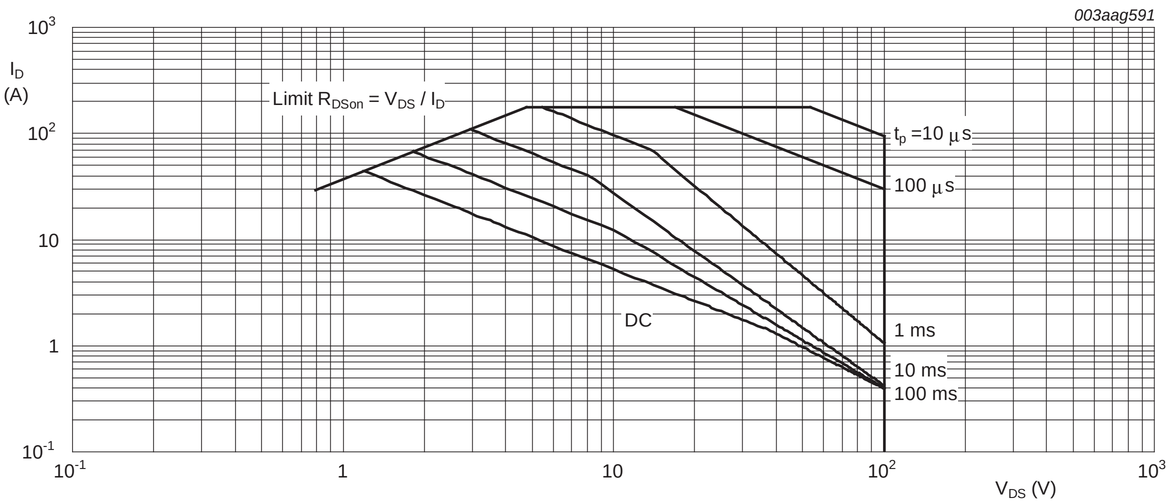


(1) $T_{j\ (init)} = 25°C$; (2) $T_{j\ (init)} = 130°C$

Fig 3. Single pulse avalanche rating; avalanche current as a function of avalanche time



$T_{mb} = 25°C$; I_{DM} is a single pulse

Fig 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

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5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 5	-	2.6	2.85	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	vertical in free air	-	55	-	K/W

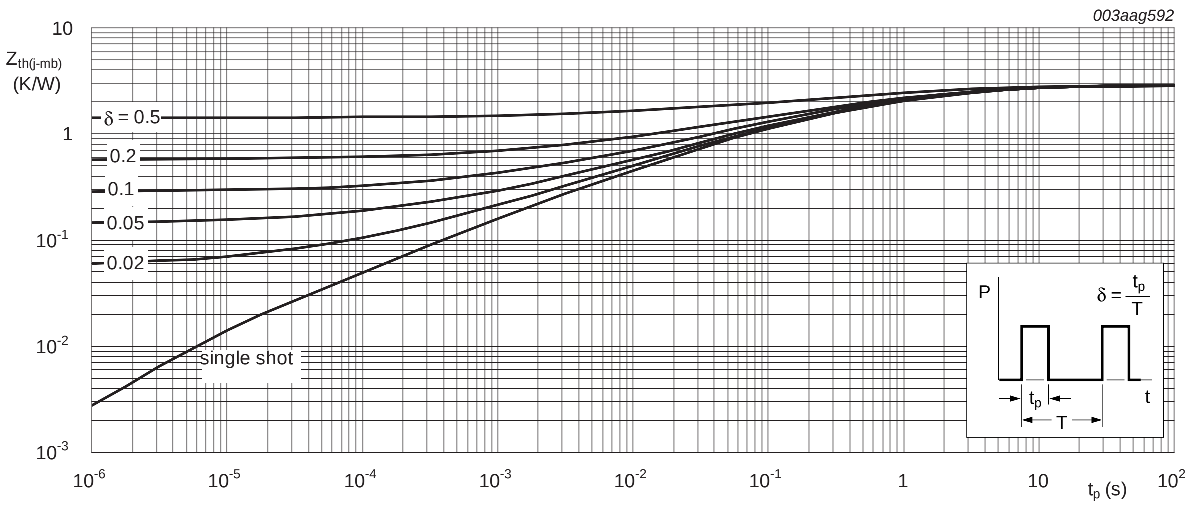

Fig 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Isolation characteristics

Table 6. Isolation characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{isol}	isolation capacitance	[1]	-	10	-	pF
$V_{isol(RMS)}$	RMS isolation voltage	50 Hz ≤ f ≤ 60 Hz; RH ≤ 65 %; sinusoidal waveform; clean and dust free	-	-	2500	V

[1] f = 1 MHz

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7. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C	100	-	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C	90	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25 °C; see Figure 10; see Figure 11	2	3	4	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = 175 °C; see Figure 10	1	-	-	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = -55 °C; see Figure 10	-	-	4.6	V
I_{DSS}	drain leakage current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C	-	-	4	µA
		V_{DS} = 100 V; V_{GS} = 0 V; T_j = 100 °C	-	-	80	µA
I_{GSS}	gate leakage current	V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 °C	-	2	100	nA
		V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 °C	-	2	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 10 A; T_j = 25 °C; see Figure 12; see Figure 13	-	8.15	9.6	mΩ
		V_{GS} = 10 V; I_D = 10 A; T_j = 100 °C; see Figure 13	-	14.25	16.8	mΩ
		V_{GS} = 10 V; I_D = 10 A; T_j = 175 °C; see Figure 13	-	22.8	26.9	mΩ
R_G	internal gate resistance (AC)	f = 1 MHz	-	0.7	-	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	I_D = 10 A; V_{DS} = 50 V; V_{GS} = 10 V; see Figure 14; see Figure 15	-	81.5	-	nC
Q_{GS}	gate-source charge		-	15.6	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	11.9	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	3.7	-	nC
Q_{GD}	gate-drain charge		-	24.3	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	I_D = 10 A; V_{DS} = 50 V; see Figure 14; see Figure 15	-	4	-	V
C_{iss}	input capacitance	V_{DS} = 50 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; see Figure 16; see Figure 17	-	4454	-	pF
C_{oss}	output capacitance	V_{DS} = 50 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; see Figure 16	-	302	-	pF
C_{rss}	reverse transfer capacitance	V_{DS} = 50 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; see Figure 16; see Figure 17	-	185	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 50 V; R_L = 5 Ω; V_{GS} = 10 V; $R_{G(ext)}$ = 4.7 Ω; T_j = 25 °C	-	21	-	ns
t_r	rise time		-	22	-	ns
$t_{d(off)}$	turn-off delay time		-	68	-	ns
t_f	fall time		-	33	-	ns

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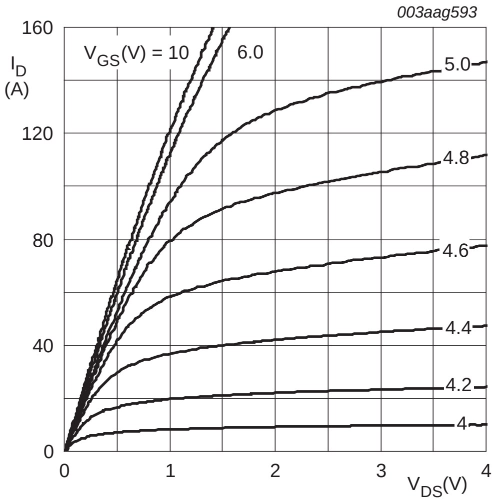
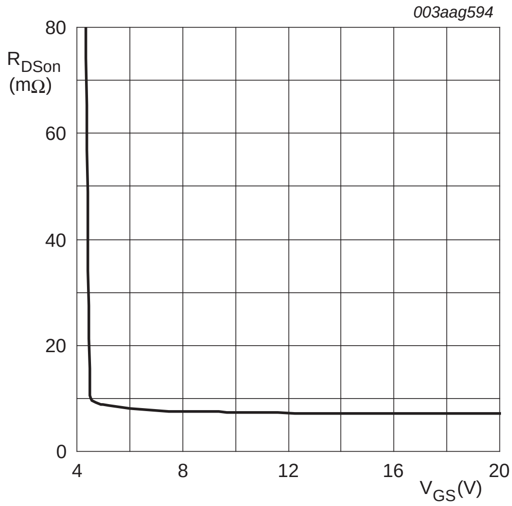
Table 7. Characteristics *...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
V_{SD}	source-drain voltage	I_S = 10 A; V_{GS} = 0 V; T_j = 25 °C; see Figure 18	-	0.76	1.2	V
t_{rr}	reverse recovery time	I_S = 10 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 50 V	-	61.5	-	ns
Q_r	recovered charge		-	157	-	nC



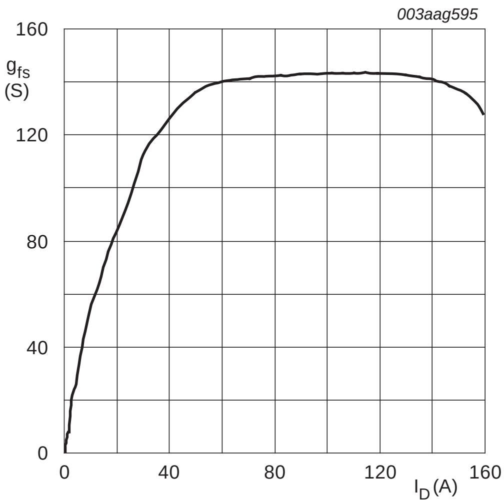
$T_j = 25°C$

Fig 6. Output characteristics; drain current as a function of drain-source voltage; typical values



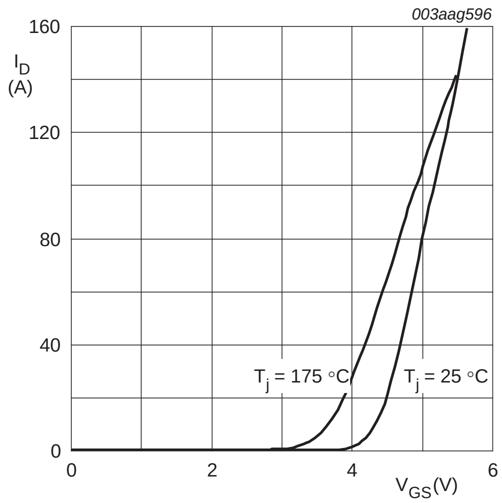
$T_j = 25°C;\ I_D = 10A$

Fig 7. Drain-source on-state resistance as a function of gate-source voltage; typical values



$T_j = 25°C;\ V_{DS} = 15V$

Fig 8. Forward transconductance as a function of drain current; typical values



$V_{DS} = 15V$

Fig 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

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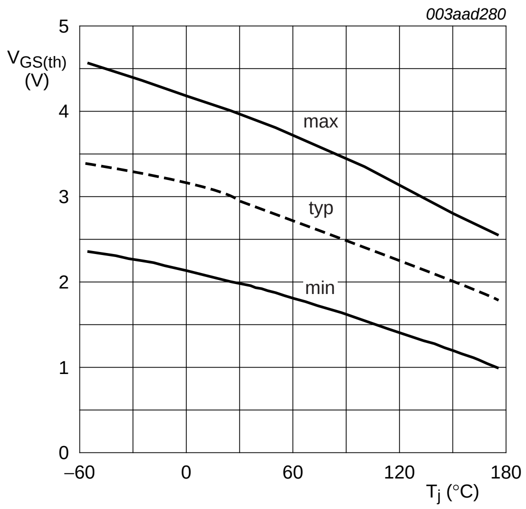
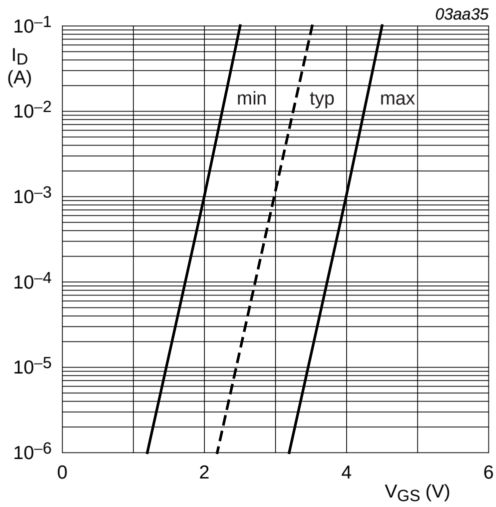


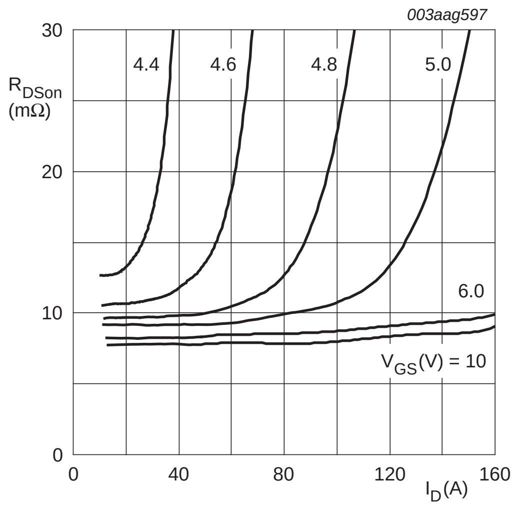
$I_D = 1\,\text{mA};\ V_{DS} = V_{GS}$

Fig 10. Gate-source threshold voltage as a function of junction temperature



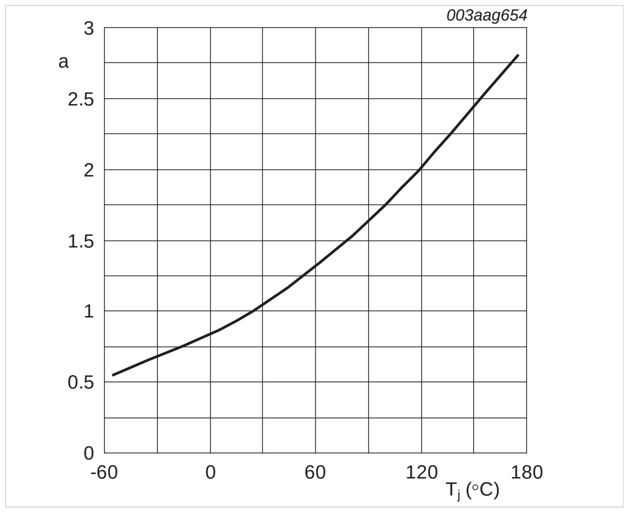
$T_j = 25\,°C; V_{DS} = 5V$

Fig 11. Sub-threshold drain current as a function of gate-source voltage



$T_j = 25°C$

Fig 12. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig 13. Normalized drain-source on-state resistance factor as a function of junction temperature

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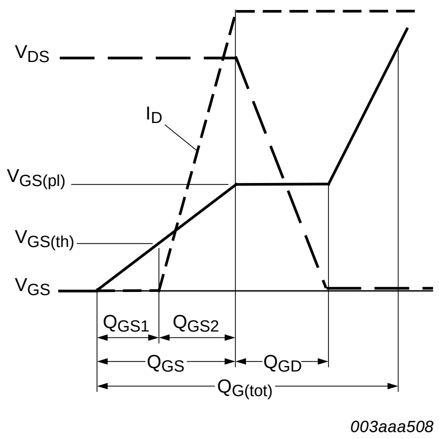
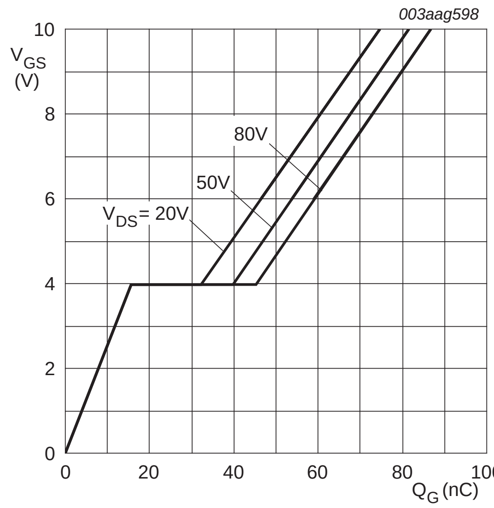
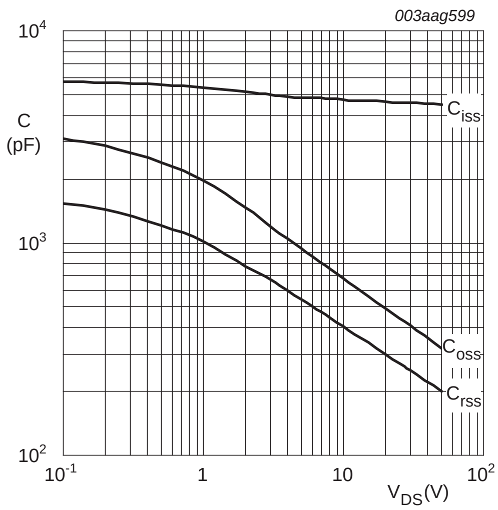


Fig 14. Gate charge waveform definitions



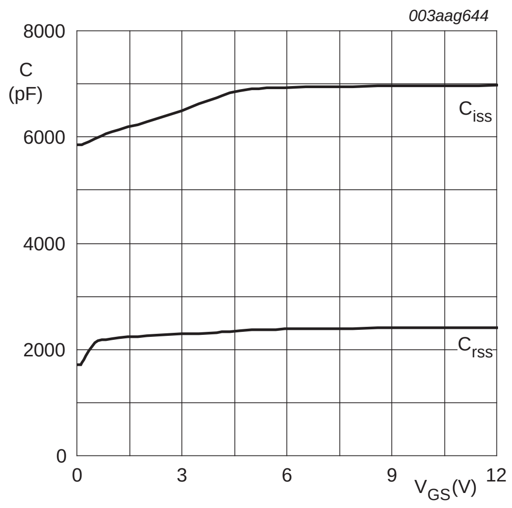
$T_j = 25°C;\ I_D = 10A$

Fig 15. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0V;\ f = 1MHz$

Fig 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$f = 1MHz;\ V_{DS} = 0V$

Fig 17. Input and reverse transfer capacitances as a function of gate-source voltage, typical values

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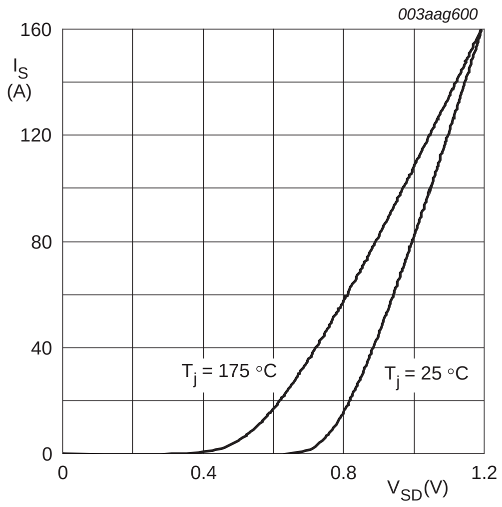

$$V_{GS} = 0V$$

Fig 18. Source current as a function of source-drain voltage; typical values

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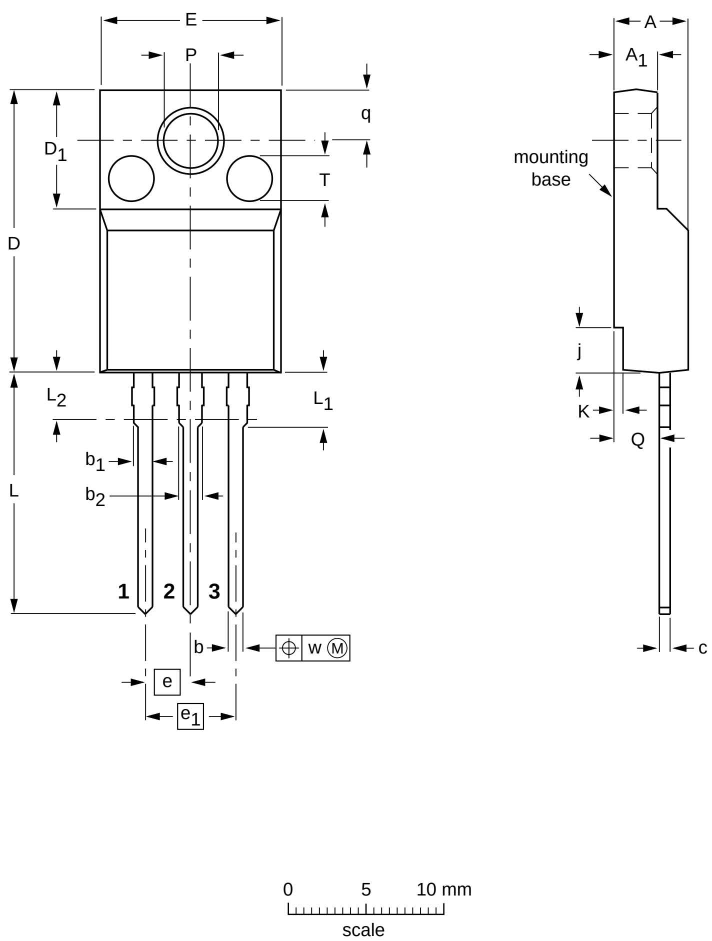
8. Package outline

Plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3-lead TO-220 'full pack'

SOT186A



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	b_1	b_2	c	D	D_1	E	e	e_1	j	K	L	L_1	L_2(1) max.	P	Q	q	T(2)	w
mm	4.6 4.0	2.9 2.5	0.9 0.7	1.1 0.9	1.4 1.0	0.7 0.4	15.8 15.2	6.5 6.3	10.3 9.7	2.54	5.08	2.7 1.7	0.6 0.4	14.4 13.5	3.30 2.79	3	3.2 3.0	2.6 2.3	3.0 2.6	2.5	0.4

Notes

1. Terminal dimensions within this zone are uncontrolled.
2. Both recesses are ∅ 2.5 × 0.8 max. depth

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT186A		3-lead TO-220F				~~02-04-09~~ 06-02-14

Fig 19. Package outline SOT186A (TO-220F)

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9. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN9R5-100XS v.3	20120306	Product data sheet	-	PSMN9R5-100XS v.2
Modifications:	• Status changed from preliminary to product. • Various changes to content.			
PSMN9R5-100XS v.2	20111020	Preliminary data sheet	-	PSMN9R5-100XS v.1

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10. Legal information

10.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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12. Contents

1 Product profile 1
1.1 General description 1
1.2 Features and benefits 1
1.3 Applications 1
1.4 Quick reference data 1
2 Pinning information 2
3 Ordering information 2
4 Limiting values 3
5 Thermal characteristics 5
6 Isolation characteristics 5
7 Characteristics 6
8 Package outline 11
9 Revision history 12
10 Legal information 13
10.1 Data sheet status 13
10.2 Definitions 13
10.3 Disclaimers 13
10.4 Trademarks 14
11 Contact information 14

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